NG-Ultra validation and on-board processing board development

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AGENDA

Context

NG-Ultra development

OLYMPE processing board

Use cases

Conclusion

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Context

- New generation spacecraft's, by the middle of the decennie will require a new level of computing processing capabilities
- Still, the mission critical elements will be made of rad-hard components which only can offer the necessary availability in the space environment
- Airbus and its partners are engaged in the development of the new very high performance System On Chip (SoC) NG-Ultra
- Beyond the chip itself, Airbus is active in developing the hardware, the software and the surrounding technologies to enable the capabilities of the NG-Ultra on competitive new generation of satellites

- With the support of ESA and the CNES, Airbus is developping a NG-Ultra flight demonstrator board

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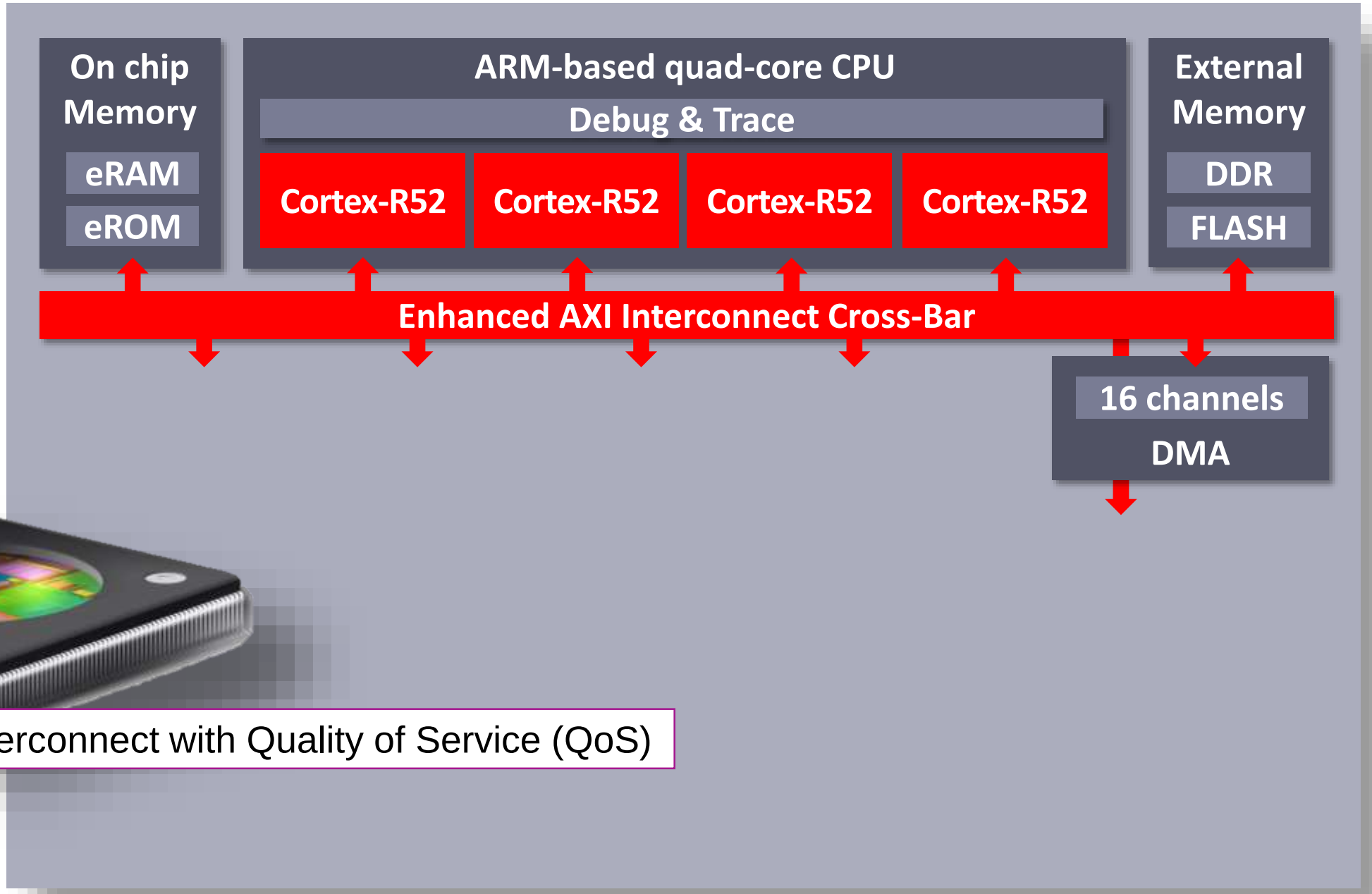
Features

- Quad-Core ARM R52 @ 600 MHz → > 7000 DMIPS
- Full compatibility with ARM Debug & Trace ecosystem

Features

- Boot eROM + 2 MBytes eRAM
- Memory interface (volatile) → DDR2/DDR3/DDR4
- Memory interface (non volatile) → Boot Flash
- 16 x channels DMA to help managing memory transfers

Features



- AXI network interconnect with Quality of Service (QoS)

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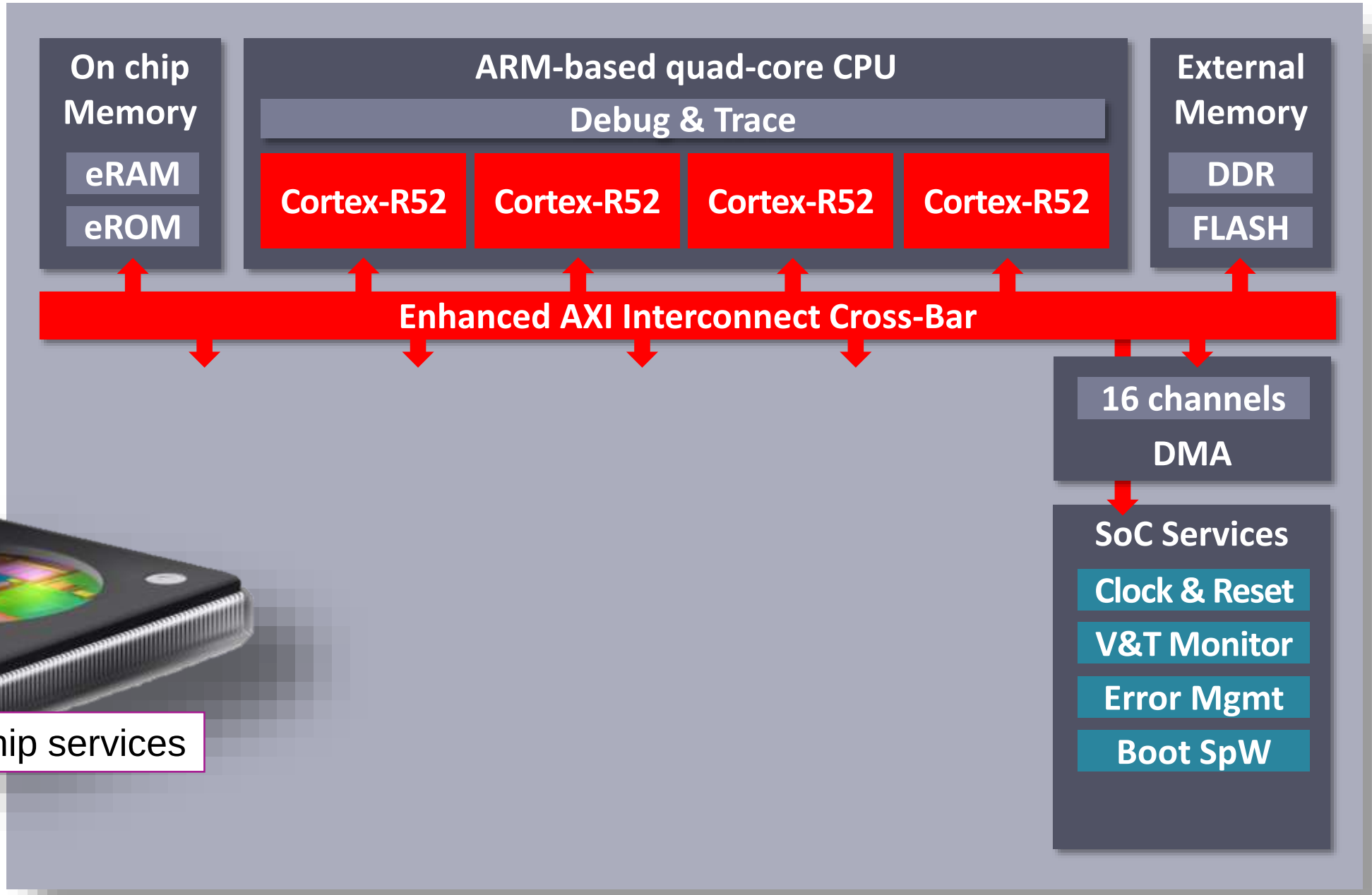
Features

- Additional on-chip services



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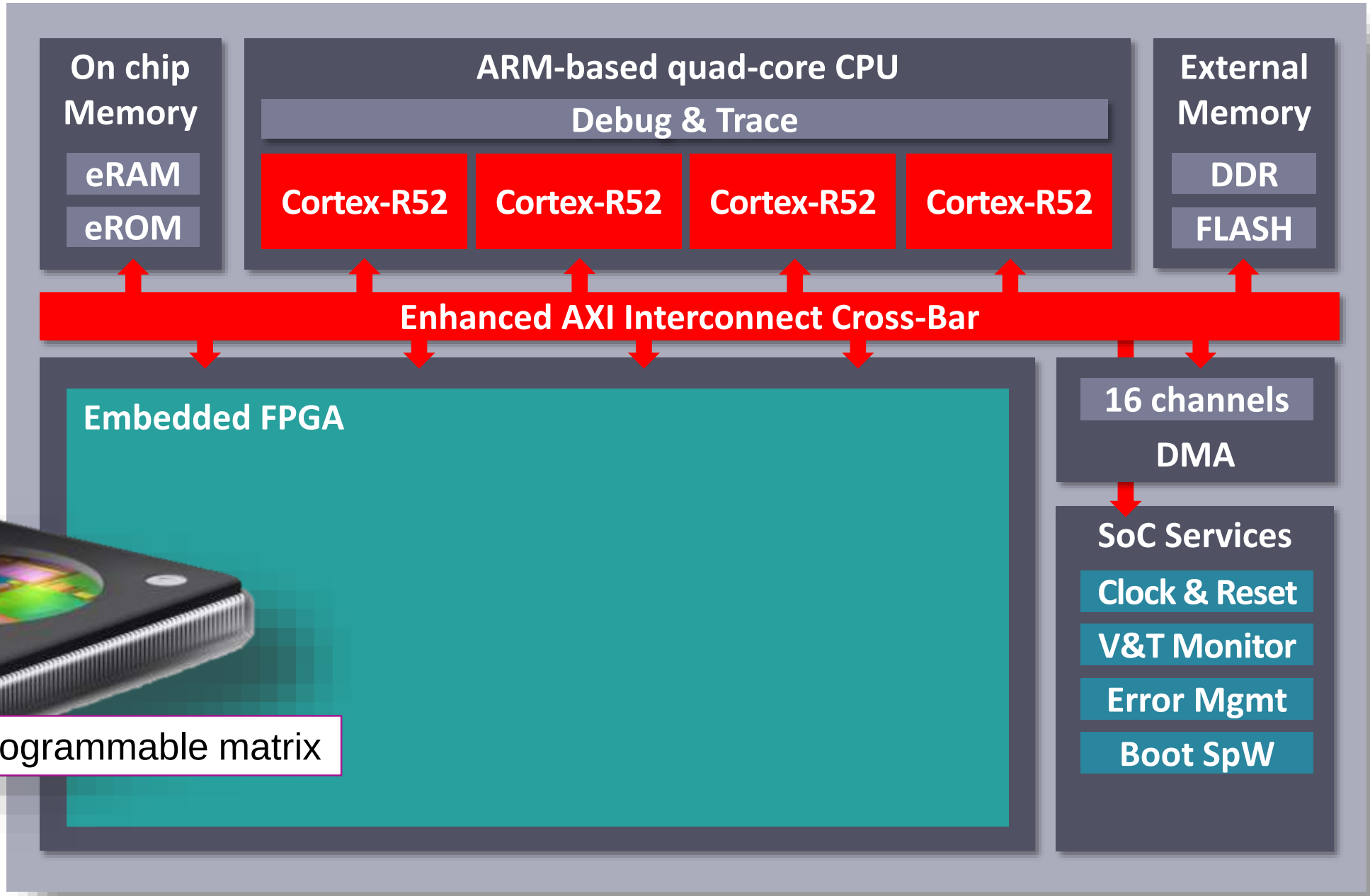
Features



- > 500 KLUTs programmable matrix

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Features

- Security features (e.g. bitstream encryption)

On chip Memory
eRAM
eROM

ARM-based quad-core CPU
Debug & Trace
Cortex-R52
Cortex-R52
Cortex-R52
Cortex-R52

External Memory
DDR
FLASH

Enhanced AXI Interconnect Cross-Bar

Embedded FPGA

16 channels
DMA

SoC Services
Clock & Reset
V&T Monitor
Error Mgmt
Boot SpW
Security

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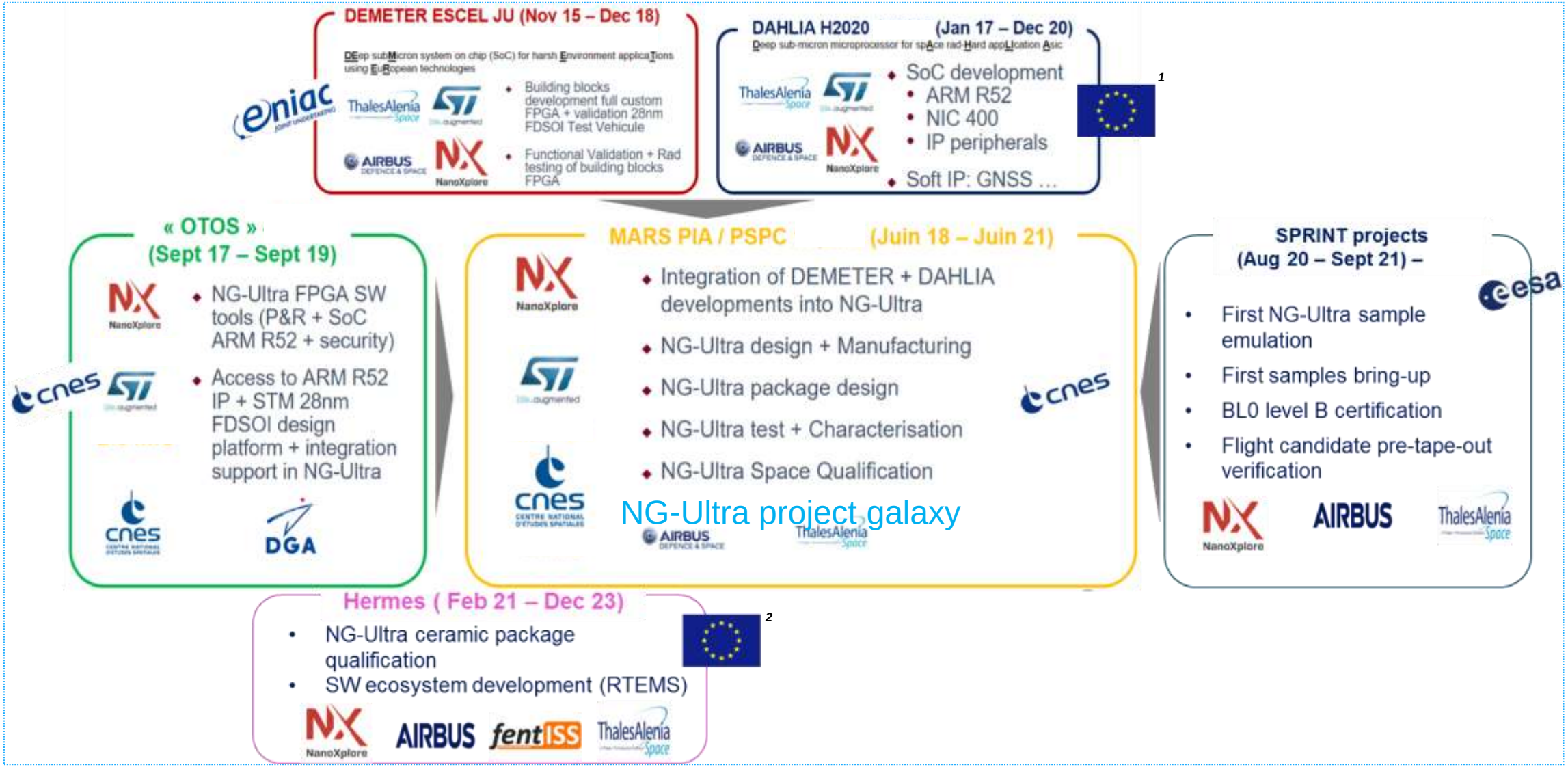
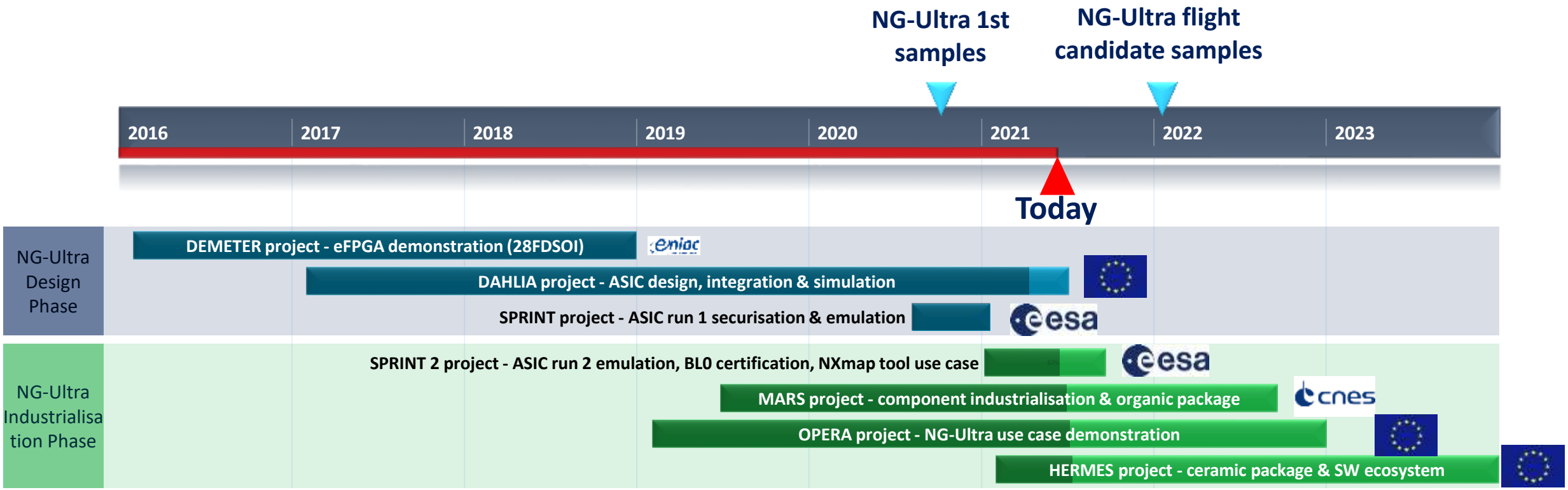
NG-Ultra: Multiple projects to support the development



[1] *This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 730011*
[2] *This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004203*

NG-Ultra Development



- Design phase is completed, performances meeting requirement specification
- Industrialisation on-going, flight sample manufacturing in 2021, component flight qualification in 2022
- First Radiation Hardened European System on Chip with eFPGA to be released on the market shortly thanks to NanoXplore, all consortium members and to the support of the agencies

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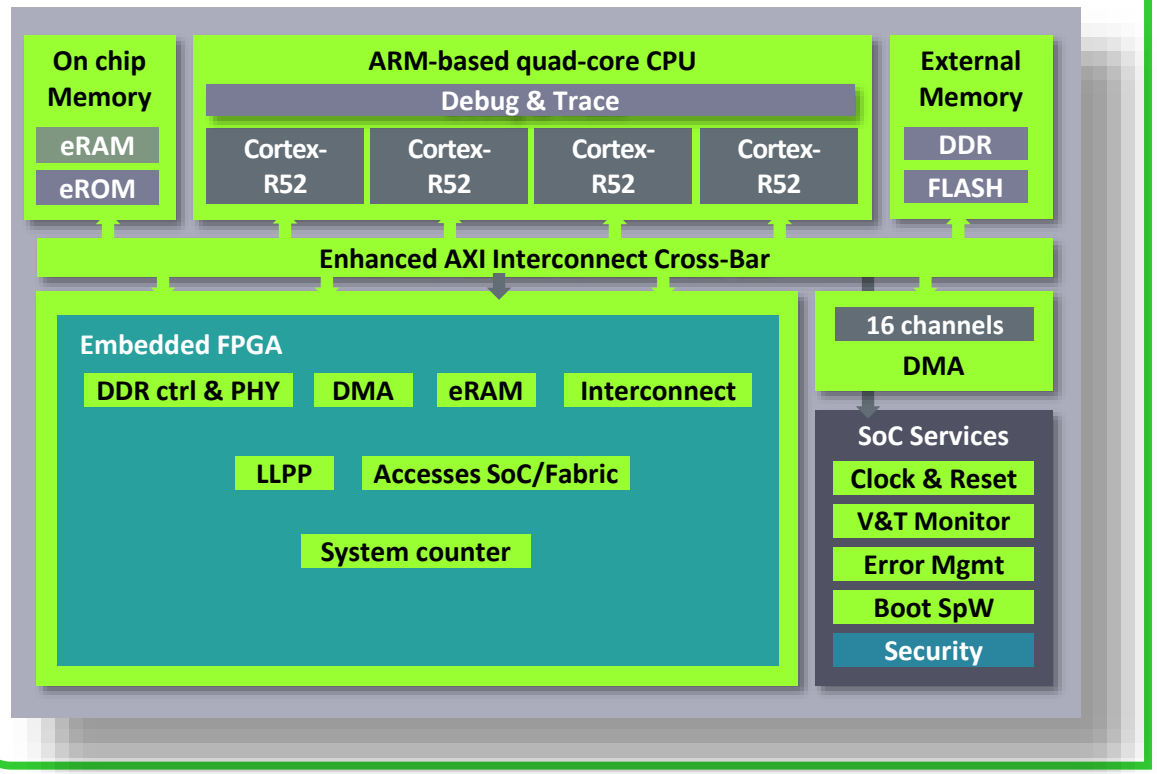
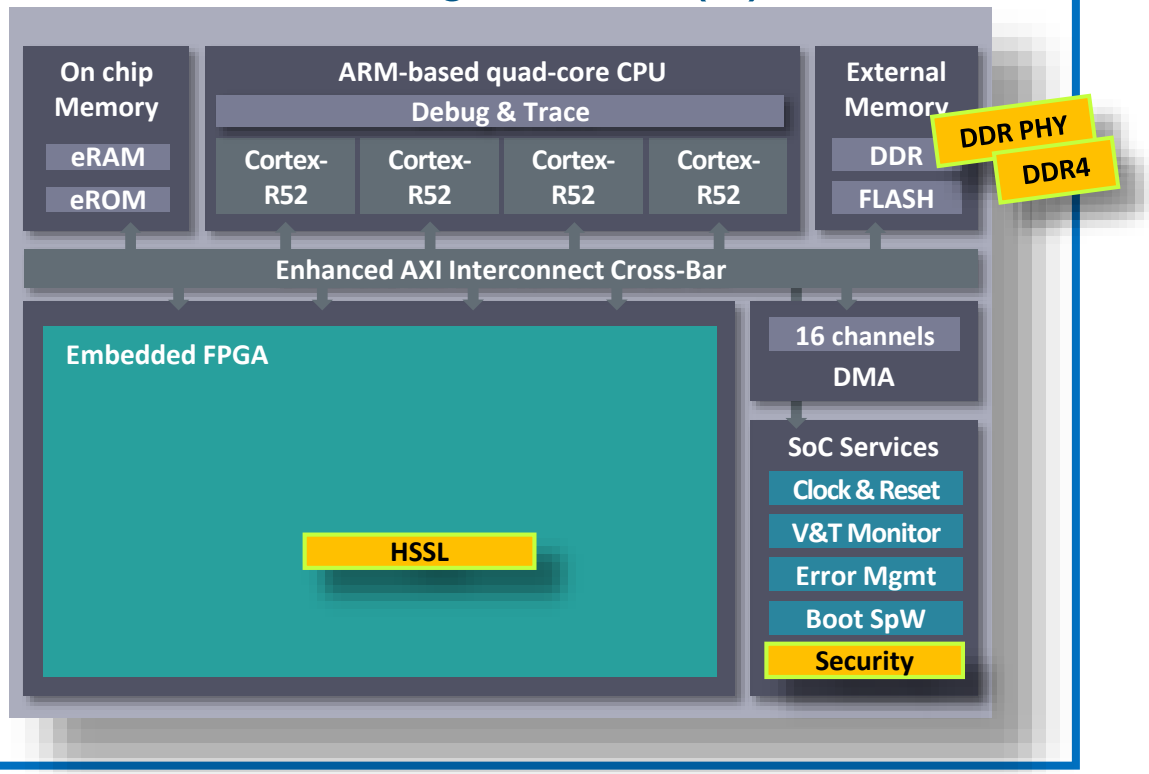
NG-Ultra validation

Proven functionalities (*)



Remaining features (**)



(*) Proven functionalities are functionalities that the consortium has been able to activate on the NG-Ultra v1 (the *real* chip on the demo board)

(**) Remaining features are functionalities not tested on the NG-Ultra v1 demo board

- DDR4 interface not tested on board since the demo board implement DDR2, but DDR has been intensively verified by simulations
- Security features (such as bitstream encryption) not tested, all tests performed in “clear” mode
- HSSL test will be fully validated by July 2021

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NG-Ultra Validation

Very regular reviews between NanoXplore, TAS and ADS with support from agencies

Exchanges on technical topics, use cases, potential issues…

- allow to share info within the consortium
- allow to improve completeness of a future user manual to benefit the European space community
- allow to take decision – if needed – on design update or workaround
- Review of FPGA place and route tool performances

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NG-Ultra processing board

- Board designed to fit ADHA standard with cPCI-ss interface
- and 12 V power interface.

- PCB designed to cope with HSSL links up to 6 Gbits/s and DDR memory

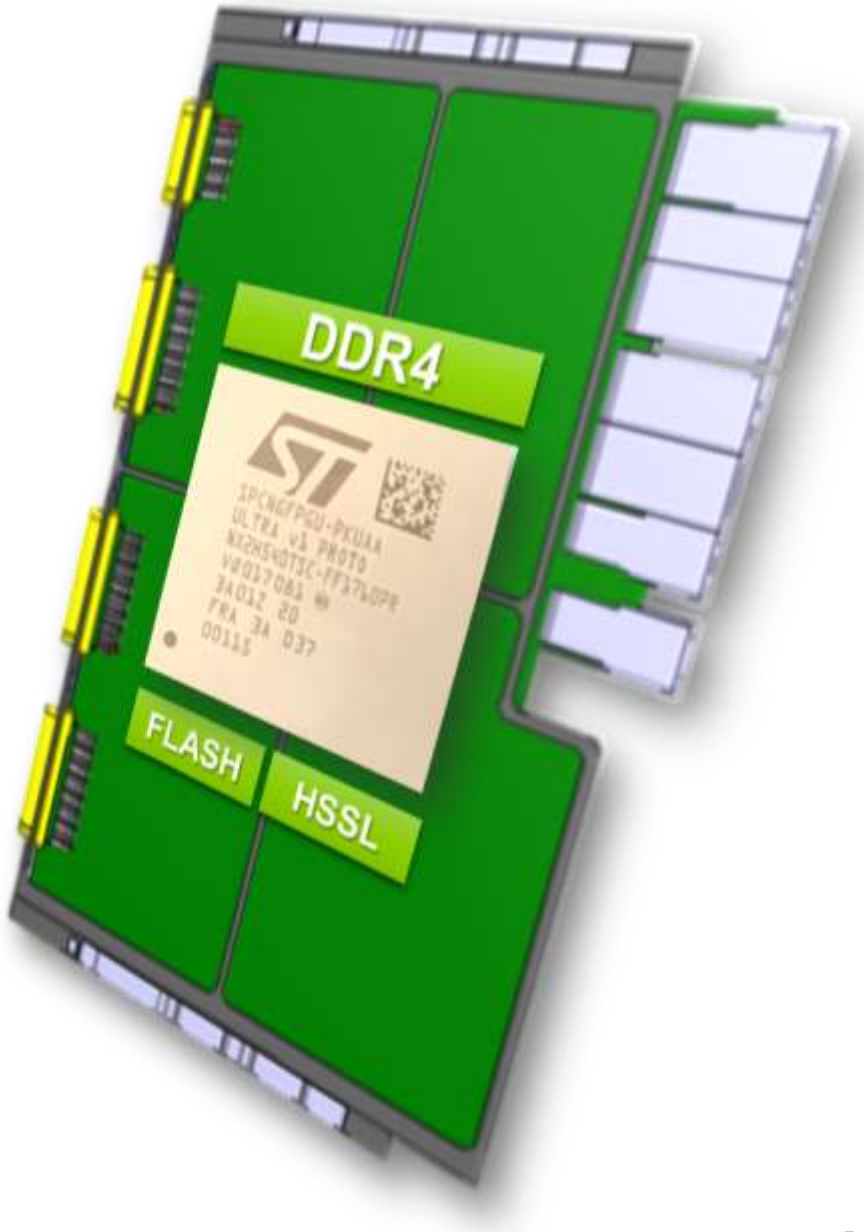
- Designed with space rad-hard EEE

- Development of OBC FPGA IPs with space constraints

- Development of SW BSP with space quality level

- Development of back panel board to interface test bench

- Validation of NG-Ultra key performances with specific applicative SW and associated test bench



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OLYMPE processing board GSTP goals

- **Validate the critical features of the NG ultra SOC**
  - High speed links
  - Exchanges with memories
  - Internal exchanges between the ARM cores and the eFPGA matrix
  - Enabling the high multi-core performances
- **Assess the development framework on a real use case**
- **Targets ADHA**, and provides inputs to the ADHA standard definiton working group

The OLYMPE processing board is the 1st iteration of the next generation OBCs

- Global architecture of OBC is analyzed to get the final split of features per board
- Form factor and interfaces are the final ones of an OBC product
- FPGA and SW features are following flight standard

OLYMPE board schedule

▪ Architecture, design, layout	Completed
▪ PDR	Completed
▪ Olympe PCB and board maufacturing	Q2 2021
▪ Integration tests	Q3-Q4 2021
▪ Demonstration of key features	Q1 2022

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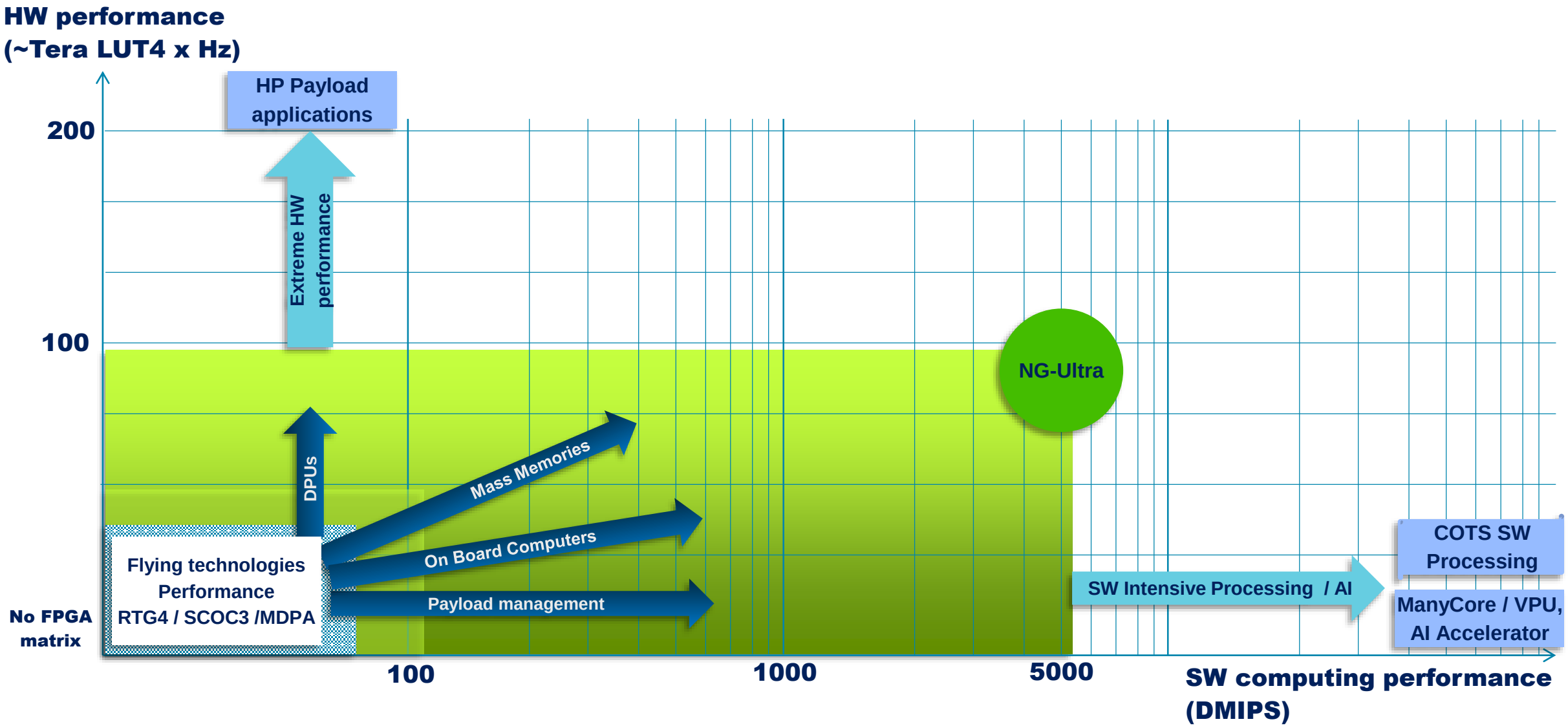
A processing element for the critical misson applications



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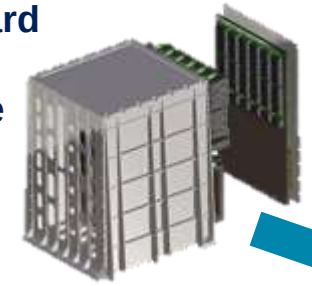
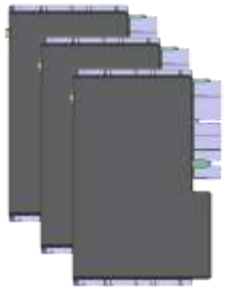
One step toward ADHA

Rack & backplane standard
Baseline :
- ADHA cPCI Serial Space
- 6U form factor primarily
- Up to 9 slots
- HSSL

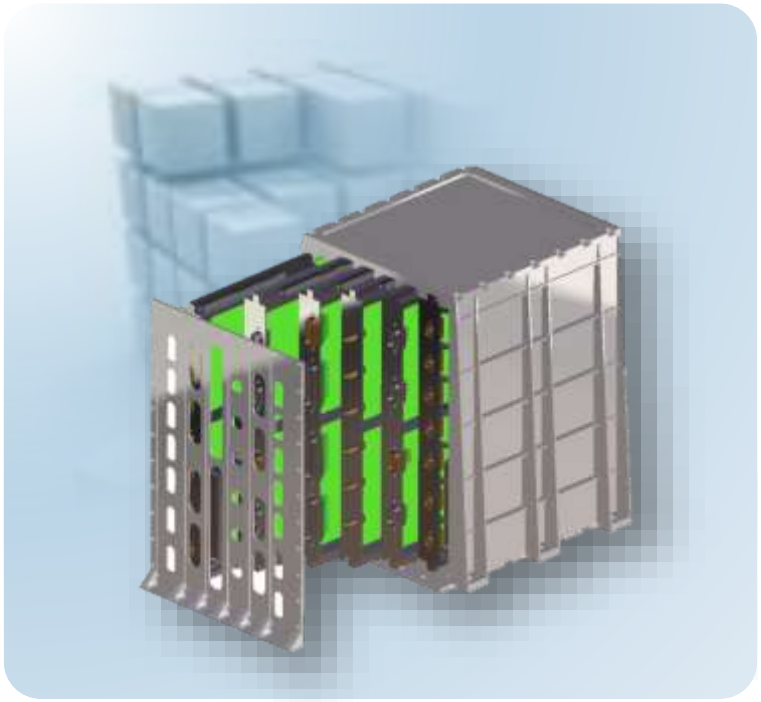


Processing Modules
- PM-Ultra
  NG-Ultra SOC

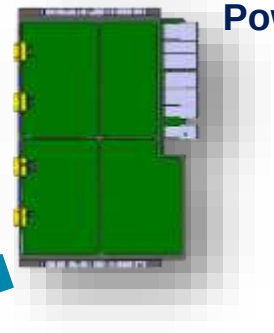
Evolutions
- COTS HP processing
- AI Accelerator



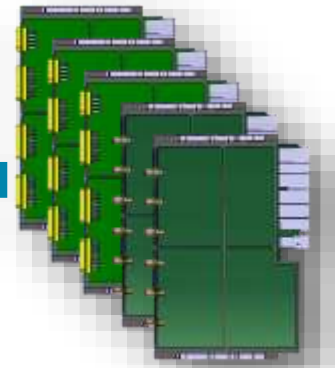
Third party modules
- Airbus partners modules
- ADHA compliant modules



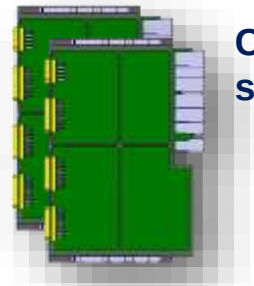
Power module



Functions module for unified avionics
- I/O controls
- GNSS
- Mass Memory
- Thermal control
- ADC/DAC



Custom modules, specific per application



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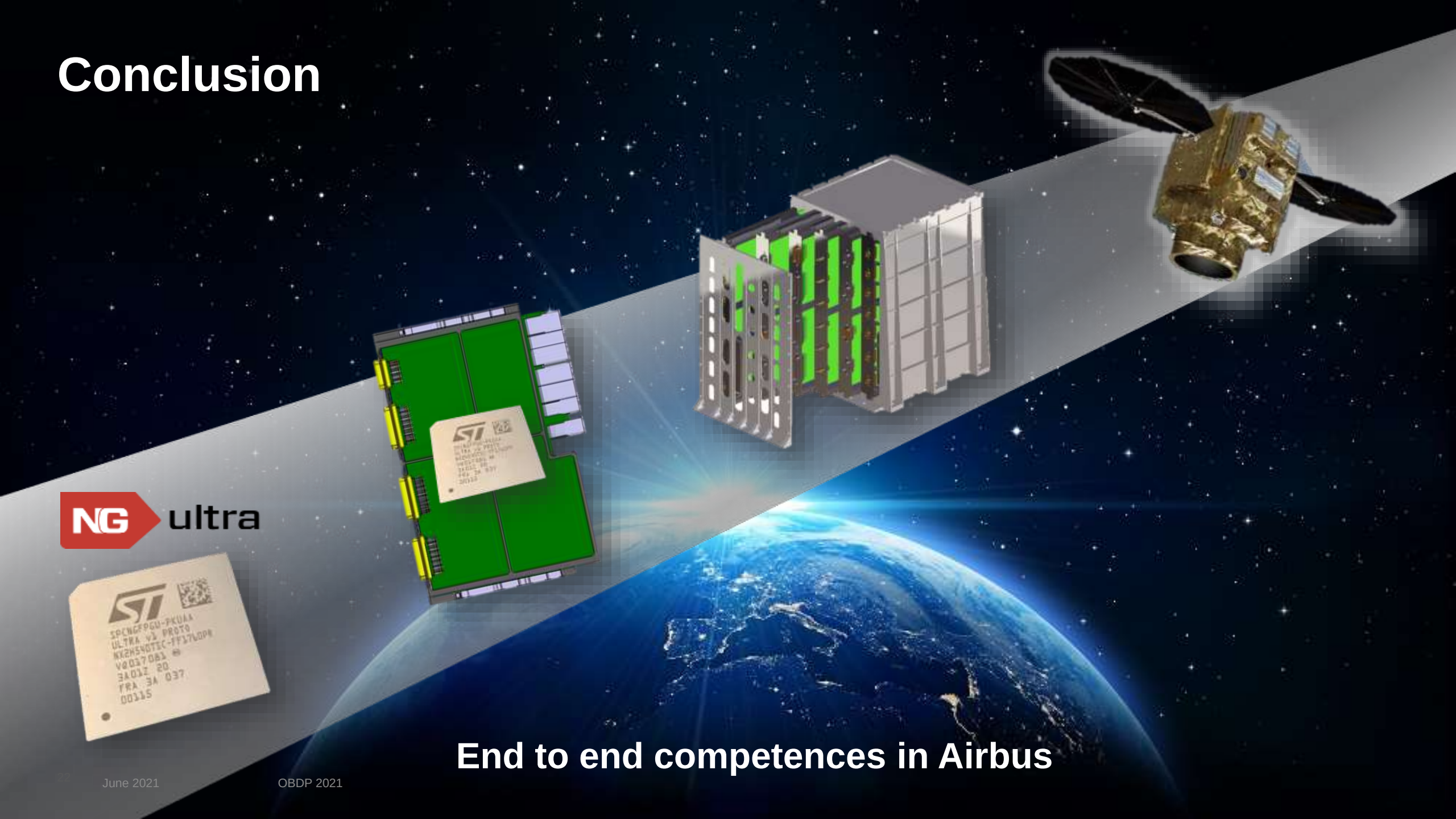

End to end competences in Airbus

Thanks to the agencies for their support

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